WHAT IS CLAIMED IS:

1. A phase detector multiplier and weighting circuit configured to multiply an analog value related to a phase difference between a bitstream and a receiver clock, comprising:

an integrator circuit configured to integrate samples of the bitstream and to generate corresponding integration-related analog values at least partly in response to phase signals derived from the receiver clock;

a weighting circuit configured to generate corresponding digital multiplicands for the corresponding integration-related analog values, wherein the digital multiplicands values are determined at least in part by the logic values of corresponding bitstream samples being integrated; and

a multiplier circuit that multiplies the digital multiplicands and the corresponding integration-related analog values to generate corresponding results indicative of a phase shift direction of the receiver clock relative to the bitstream.

2. The phase detector multiplier and weighting circuit as defined in Claim 1, wherein multiplicands for corresponding integration-related analog values larger than a first amount have a value of zero.

3. The phase detector multiplier and weighting circuit as defined in Claim 1, wherein the multiplier is configured to selectively couple the integration circuit to a constant current circuit to thereby generate the corresponding results.

4. The phase detector multiplier and weighting circuit as defined in Claim 1, wherein the weighting circuit is configured to generate control signals used selectively activate corresponding stages of the multiplier circuit.

5. The phase detector multiplier and weighting circuit as defined in Claim 1, wherein the corresponding results are used to generate phase error signals.

6. The phase detector multiplier and weighting circuit as defined in Claim 1, wherein the phase detector multiplier and weighting circuit is fabricated from silicon-germanium.

7. The phase detector multiplier and a weighting circuit as defined in Claim 1, wherein each of the multiplicands generated by the weighting circuit is one of

a first predetermined multiplicand value, a negative of the first predetermined multiplicand value, and zero.

8. A two-stage phase detector multiplier circuit used to detect a phase error between a first clock and serial data, comprising:

a first stage circuit configured to provide a corresponding multiplicand for a corresponding analog phase difference-related value, the corresponding analog phase difference-related value used to indicate at least in part the phase difference between the first clock and the serial data, wherein the multiplicand value is determined at least in part by logical states of a corresponding plurality of serial data bits; and

a second stage circuit coupled to receive the multiplicand from the first stage circuit, the second stage circuit configured to multiply the multiplicand and the corresponding analog phase difference-related value to generate a first result indicative of one of a lead and a lag of the first clock relative to the serial data.

9. The two-stage phase detector multiplier circuit as defined in Claim 8, wherein the first stage is configured to determine whether adjacent bits in the serial data have the same logical value.

10. The two-stage phase detector multiplier circuit as defined in Claim 8, wherein the first stage is configured to determine whether adjacent bits in the serial data have different logical values.

11. The two-stage phase detector multiplier circuit as defined in Claim 8, wherein the second stage includes an inverting output and a non-inverting output, wherein each of the inverting output and a non-inverting output is selectively coupleable to at least a first integration storage element used to generate the analog phase difference-related value.

12. A method of multiplying an analog phase difference-related value by a multiplicand, the method comprising:

generating a multiplicand for a corresponding analog phase difference-related value, the corresponding analog phase difference-related value used to indicate at least in part the phase difference of a first clock and a serial data

stream, wherein the multiplicand value is determined at least in part by logical states of a corresponding plurality of serial data stream bits used to generate the analog phase difference-related value; and

multiplying the corresponding analog phase difference-related value by the corresponding multiplicand to generate a first result indicative of one of a lead and a lag of the first clock relative to the serial data stream.

13. The method as defined in Claim 12, wherein the analog phase difference-related value is an integration value obtained by integrating over a sample of the corresponding plurality of serial data bits.

14. The method as defined in Claim 12, wherein the multiplicand is one of three predetermined values.

15. The method as defined in Claim 12, further comprising receiving the serial data over a network interface.

16. The method as defined in Claim 12, wherein the corresponding plurality of serial data stream bits includes two adjacent serial data stream bits.

17. A network interface circuit, comprising:

a first network interface port configured to receive a bitstream from a network;

a first multiplicand circuit coupled to receive at least a first portion of the bitstream, the first multiplicand circuit configured to generate a first multiplicand value for a first corresponding analog phase difference-related value, the first corresponding analog phase difference-related value used to indicate at least in part the phase difference of a first clock and the bitstream, wherein the first multiplicand value is determined at least in part by logical states of a first corresponding plurality of bitstream bits;

a first multiplier circuit coupled to the first multiplicand circuit to receive the first multiplicand value, the first multiplier circuit configured to multiply the first multiplicand value and the first corresponding analog phase difference-related value to generate a first result indicative of one of a lead and a lag of the first clock relative to the bitstream;

a second multiplicand circuit coupled to receive at least a second portion of the bitstream, the second multiplicand circuit configured to generate a second multiplicand value for a second corresponding analog phase difference-related value, the second corresponding analog phase difference-related value used to indicate at least in part the phase difference of the first clock and the bitstream, wherein the second multiplicand value is determined at least in part by logical states of a second corresponding plurality of bitstream bits;

a second multiplier circuit coupled to the second multiplicand circuit to receive the second multiplicand value, the second multiplier circuit configured to multiply the second multiplicand value and the second corresponding analog phase difference-related value to generate a second result indicative of one of a lead and a lag of the first clock relative to the bitstream; and

a summing circuit configured to sum the first result and the second result.

18. The network interface circuit as defined in Claim 17, wherein the summed first result and second result is used to generate a phase error signal that synchronizes the first clock with the bitstream.

19. The network interface circuit as defined in Claim 17, wherein the first network interface port is configured to interface with a SONET network.

20. The network interface circuit as defined in Claim 17, wherein the first corresponding plurality of bitstream bits are two adjacent bitstream bits.

21. The network interface circuit as defined in Claim 17, wherein the network interface circuit is fabricated from silicon-germanium.